A Realistic Large-Signal MESFET Model for SPICE

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***Abstract*—A comprehensive large-signal MESFET model that provides a realistic description of measured characteristics over all operating regions is presented. It describes subthreshold conduction and breakdown. It has frequency dispersion of both transconductance and drain conductance, and derates with power dissipation. All derivatives are continuous for a realistic description of circuit distortion and intermodulation. The model has improved descriptions of capacitance and bias dependence. It has small-signal S-parameter accuracy extended to a wide range of operating conditions. The model is implemented with new techniques for continuity and dispersion. These provide accurate prediction of circuit performance and also improve simulation speed.**

***Index Terms*—MESFET's, modeling, simulation.**

I. Introduction

THE MODEL developed in this paper has been designed to provide an accurate description of GaAs MESFET's in large-signal RF applications and communication circuits. The model is continuous for accurate harmonic distortion analysis, frequency dependence, and independent characterization of various operating regions.

For accurate harmonic and large-signal analysis, a description with high-order continuity is essential. The equations used must maintain strict continuity in their high-order derivatives over all terminal potentials. In general, established MESFET models have discontinuous empirical simplifications that compromise their accuracy. Several are based on the hyperbolic tangent description [1]–[3]. This is not accurate in the controlled-resistance region, in which these models predict incorrect drain conductance. Giving dependence on gate bias to the knee potential improves this [4], but an increased third-order component observed in the knee region is not predicted. The proposed solution is to start with a classic model of FET operation in the controlled-resistance region and modify it to describe controlled-current operation due to velocity saturation.

The prediction of distortion has been improved by using higher order descriptions of the transfer characteristic. Several models use cubic [5] and general power laws [6]. However, most omit subthreshold conduction and have a conditional cutoff. Others use a separate exponential description with an abrupt transition from normal mode to cutoff mode [7], [8]. There is always a nonphysical discontinuity in high-order derivatives associated with the transition to cutoff. Other models maintain well-defined derivatives, such as [9] for MOSFET's and [10] for HEMT's and MESFET's. The latter does not handle frequency-dispersion effects, which are significant in MESFET's. The model presented here uses a nested transformation technique to include subthreshold current within a continuous function [11]. This gives superior accuracy that extends to the normal operating region [12].

Anomalous rate-dependent behavior is also a primary consideration in MESFET modeling. Several models implement frequency-dispersion effects by incorporating extra nodes that are used to modulate the output conductance [13]–[15]. However, dispersion of both transconductance and output conductance is required. The new model describes the frequency dependence of output conductance and transconductance about any bias point in a manner that is consistent with S-parameter and pulse measurements. The extent of self-heating and dispersion effects vary with the rate of terminal excitation.

Before the development of the model, the following section identifies those elements that are extrinsic to the main description. Then the following section presents the intrinsic dc drain–source current model. The subsequent section gives details of rate dependence and frequency dispersion. Finally, the charge storage model is presented.

II. Extrinsic Model

The development of the MESFET model presented in this paper starts from the simple view of a field-effect transistor as a doped semiconductor channel between source and drain terminals. This channel is controlled by depleting the region under a gate electrode with a gate–source bias, $v_{\rm GS}$. The device operates in three modes. In the controlled-resistance mode, the drain–source current $i_{\rm DS}$ is proportional to the drain–source voltage, $v_{\rm DS}$. As $v_{\rm DS}$ increases, the device enters the controlled-current mode where the drain current ceases to rise with drain potential because at the drain end, the channel is completely depleted, or pinched off. The third mode is cutoff, where no current flows because the channel is depleted at the source end.

The FET model, shown in Fig. 1, is more comprehensive. Electrical connection to the source and drain terminals is via ohmic resistance elements with values R_S and R_D. These resistances are independent of temperature and terminal potentials. Correct determination of these resistances and subsequent de-embedding is crucial to accurate extraction of the other model parameters.

The gate electrode forms a Schottky contact, which is modeled by drain–gate and gate–source currents. The standard diode equation describes these currents with parameters I_S and N. Reverse breakdown currents, described by a similar function with parameters $I_{\rm BD}$ and $V_{\rm BD}$, are also included:

$$i_{\rm GD} = I_S[e^{v_{\rm GD}/NV_t} - 1] - I_{\rm BD}[e^{-v_{\rm GD}/V_{\rm BD}} - 1]$$
$$i_{\rm GS} = I_S[e^{v_{\rm GS}/NV_t} - 1] - I_{\rm BD}[e^{-v_{\rm GS}/V_{\rm BD}} - 1]. \quad (1)$$

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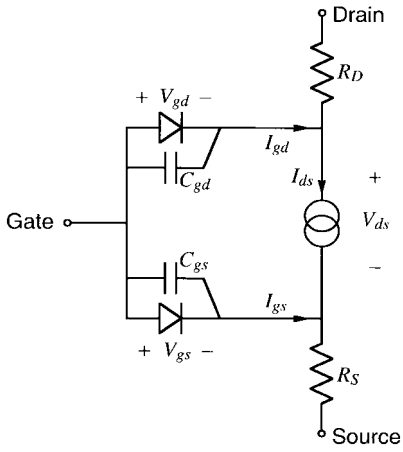

Fig. 1. Lumped-element topology of the FET model.

The forward current parameters are easily determined by fitting to measurements of gate current at zero $v_{\rm DS}$ and moderate forward gate–source bias. The breakdown parameters are determined from measurements of gate current with large negative $v_{\rm GD}$. The breakdown potential $V_{\rm BD}$ should not be confused with a data-sheet specification. The parameters are chosen to fit measurements such as shown in Fig. 2. Typical values of $V_{\rm BD}$ are less than 1 V.

Channel current from drain to source is described by an intrinsic-current source.

III. Intrinsic-Current Model

A general power-law function of effective gate and drain potentials $v_{\rm GT}$ and $v_{\rm DT}$ describes the intrinsic drain–source current with model parameters β and Q:

$$i_D = \beta v_{\rm GT}^Q [1 - (1 - v_{\rm DT}/v_{\rm GT})^Q]. \tag{2}$$

This is a description of controlled-resistance operation where $0 < v_{\rm GT} < v_{\rm DT}$. For $Q = 2$, it is the equation used in the SPICE square-law JFET model. In the cutoff mode where $v_{\rm GT} \le 0$, the original JFET model sets $i_D = 0$ and in the controlled-current mode, where $v_{\rm DT} \ge v_{\rm GT}$, it sets $i_D = \beta v_{\rm GT}^Q$.

In the new model developed in this paper, the cutoff and the controlled-current modes will be modeled using (2) by placing a restriction on the values of $v_{\rm GT}$ and $v_{\rm DT}$ such that $0 < v_{\rm GT} < v_{\rm DT}$ is always true. The important difference is that the restrictions will be implemented with smooth transform functions, which eliminate high-order discontinuities.

A. Controlled-Current Mode

The new model describes early onset of controlled-current operation in a MESFET by placing a restriction on the maximum value of $v_{\rm DT}$. Operation is considered to be in controlled-current mode when $v_{\rm DT} \ge V_{\rm sat}$ and is described by setting $v_{\rm DT} \approx V_{\rm sat}$.

The model must select $V_{\rm sat}$ to be the lesser of $v_{\rm GT}$ and the velocity saturation potential. The latter is set by parameter ξ and the channel depletion potential, $\phi_b - V_{TO}$. A smooth function selects the lesser potential

$$V_{\rm sat} = \frac{\xi(\phi_b - V_{TO}) v_{\rm GT}}{\xi(\phi_b - V_{TO}) + v_{\rm GT}}. \tag{3}$$

The terms ϕ_b and V_{TO} are the gate–junction barrier potential and the gate–source potential required to pinch off the channel, respectively. The parameter ξ has the same interpretation as in the analytic model of [16]. It is related to the product of the gate length and electric field strength required for velocity saturation. For a 1-μm GaAs MESFET, ξ is approximately 0.3.

At this point, the model is a conditional function that switches between operating modes. However, coinciding with each switch there is a discontinuity in the derivatives. This is an inherent fault in any model that uses conditional functions, in terms of distortion and intermodulation prediction.

The solution adopted here is to eliminate conditional function formulations and only describe the linear operating mode. To accomplish this, the arguments in (2) must be restricted to $v_{\rm GT} \in (0, \infty)$ and $v_{\rm DT} \in [0, V_{\rm sat})$.

A smooth transformation implements the restriction of $v_{\rm DT}$ with parameter Z, which controls the shape of the saturation knee as follows:

$$v_{\rm DT} = \tfrac{1}{2}\sqrt{(v_{\rm DP}\sqrt{1+Z} + V_{\rm sat})^2 + ZV_{\rm sat}^2} - \tfrac{1}{2}\sqrt{(v_{\rm DP}\sqrt{1+Z} - V_{\rm sat})^2 + ZV_{\rm sat}^2}. \tag{4}$$

This function maps an alternative effective drain potential $v_{\rm DP} \in [0, \infty)$ to $v_{\rm DT} \in [0, V_{\rm sat})$. For low drain potentials $v_{\rm DT} \approx v_{\rm DP}$ and at $v_{\rm DP} = 0$, the second and higher derivatives with respect to $v_{\rm DP}$ are zero. Thus, this transformation has no effect on the controlled-resistance mode description. When $v_{\rm DP}$ is large, corresponding to large drain–source potential, $v_{\rm DT} \approx V_{\rm sat}$, so (2) will describe controlled-current operation. If Z is zero then the transition is extremely sharp, but a typical value is between 0.5 and 1.5.

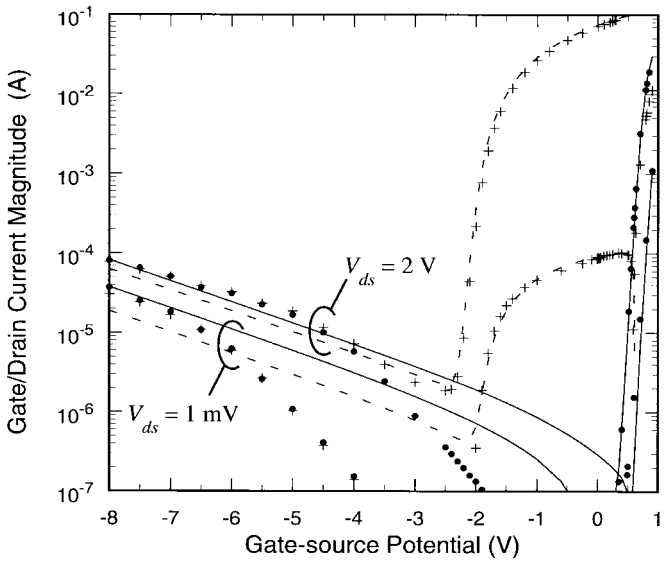

Fig. 2. Drain (+) and gate (•) current of an MGF1400 GaAs MESFET measured at drain–source potentials of 1 mV and 2.0 V. Simulated drain (- - -) and gate (——) currents were produced with parameters in (1) selected to fit the breakdown region where $v_{\rm GD} < -6.0$ V, and the forward gate–current region, $v_{\rm GS} > 0.5$ V.

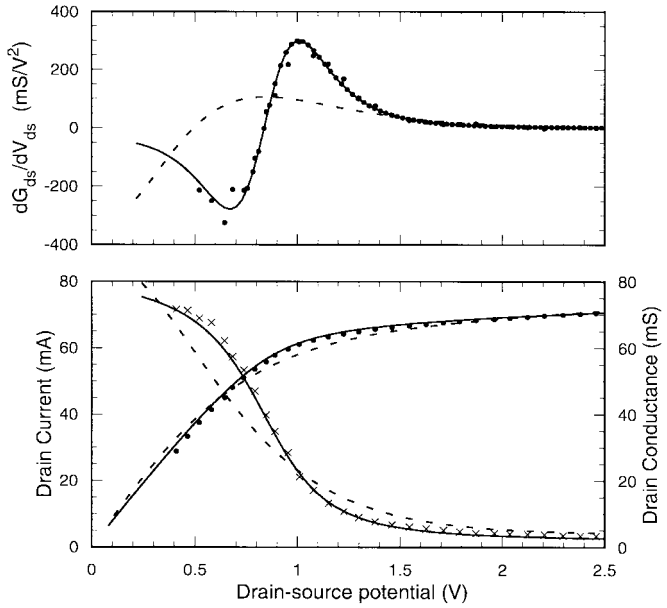

Fig. 3. Current saturation and its first and second derivatives described by the new model (——), and a hyperbolic tangent (- - -). Measured data ($\bullet$, $\times$) is also shown.

The continuity of this transformation provides a description of the transition to controlled-current operation that correctly describes drain–source conductance. Fig. 3 shows the marked improvement over the hyperbolic tangent function [1] used in several other models.

B. Dual Power Law

The model provides independent control over the power-law exponent in the controlled-resistance and the controlled-current regions. In the controlled-resistance mode, near zero drain potential, the description is a P, rather than Q power law. A mapping of the terminal drain–source potential to the effective drain potential of (4) implements this *dual* $(P-Q)$ *power law*:

$$v_{\rm DP} = v_{\rm DS}\frac{P}{Q}\left(\frac{v_{\rm GT}}{\phi_b - V_{TO}}\right)^{P-Q}. \tag{5}$$

When $v_{\rm DS}$ is large, $v_{\rm DP}$ will also be large and (4) will set $v_{\rm DT} \approx V_{\rm sat}$, so the intrinsic drain current will be described by (2) as a Q power law. In fact, for short-channel FET's, with small ξ, the modeled controlled-current characteristic is approximately proportional to $v_{\rm GT}^{Q-1}$. This is a useful assumption for estimating the parameter Q from measured transfer characteristics.

When $v_{\rm DS}$ is small, $v_{\rm DP}$ will be little changed by (4). The drain–source conductance predicted by (2) then becomes that of a P power law:

$$\left.\frac{di_D}{dv_{\rm DS}}\right|_{v_{\rm DS}=0} = Pv_{\rm GT}^{P-1}(\beta(\phi_b - V_{TO})^{Q-P}). \tag{6}$$

Typical values of P are near 2.4, which is the value that best approximates the Shockley analysis of an ideal FET [17]. This is the expected behavior in conditions of low-electric field. Experience with many different types of GaAs MESFET's has shown that values of P that are not near 2.4 have been the result of incorrect extraction of the extrinsic resistances or the pinchoff potential.

A single set of dual power-law model parameters can describe both the controlled-resistance and controlled-current regions. Drain conductance in the controlled-resistance region versus gate potential is fitted with parameter P. Transconductance in the controlled-current region is fitted with parameter Q. Typical values of Q are near 2.0 and the difference between P and Q gives the model the characteristic extended controlled-resistance region that is observed in measurements.

C. Cutoff Mode

Applying a large negative gate potential to a FET never succeeds in completely cutting off drain current. Near pinchoff, the current diminishes exponentially with gate potential and will increase when gate–drain breakdown occurs. Several models have been proposed [18], [19], but not all correctly separate drain–gate and drain–source currents. In this model, the extrinsic-current element describes drain–gate breakdown.

Diminishing intrinsic drain current is described by a smooth transformation that restricts the value of the term $v_{\rm GT}$ in (2). The intrinsic drain–source current is never allowed to completely cut off:

$$v_{\rm GT} = V_{\rm ST}(1+M_{\rm VST}v_{\rm DS}) \cdot \ln\left(1+\exp\left(\frac{v_{\rm GST}}{V_{\rm ST}(1+M_{\rm VST}v_{\rm DS})}\right)\right). \tag{7}$$

This function maps the effective gate potential relative to the channel pinchoff potential, $v_{\rm GST} \in (-\infty, \infty)$, to $v_{\rm GT} \in (0, \infty)$. If $v_{\rm GST} \gg V_{\rm ST}$ then $v_{\rm GT} \approx v_{\rm GST}$ and (7) has no effect on the model. On the other hand, if $v_{\rm GST} \ll V_{\rm ST}$ then $v_{\rm GT}$ is proportional to the logarithm of a quantity slightly larger than unity. In this case $v_{\rm GT}$ will then be proportional to the exponential of $v_{\rm GST}$.

The terms $M_{\rm VST}$ and $V_{\rm ST}$ are model parameters that can be understood by substitution of (7) into (2). For small $v_{\rm GT}$, the logarithm of drain current in controlled-current mode is a linear function of $v_{\rm GST}$:

$$\frac{d\ \log(i_D)}{dv_{\rm GST}} = \frac{Q\ \log(e)}{V_{\rm ST}(1+M_{\rm VST}v_{\rm DS})}. \tag{8}$$

This region is clearly visible in Fig. 2, which used $V_{\rm ST} = 65$ mV and $M_{\rm VST} = 0.12\ {\rm V}^{-1}$.

There is some interaction between the subthreshold model parameters and the pinchoff potential, which includes frequency-dispersion and drain-feedback terms described in the following section.

The transformation of $v_{\rm GST}$, like the other transformations in the model, is well behaved and infinitely differentiable. Derivatives of the model remain continuous. Fig. 4 shows the resulting third-order derivative. It provides a superior prediction of measurement and thus, it can describe intermodulation distortion realistically [12]. The phase of third-order components in the normal-mode region is accurately described by this model and matches results obtained from S-parameter measurements [20]. Fig. 5 shows simulated and measured

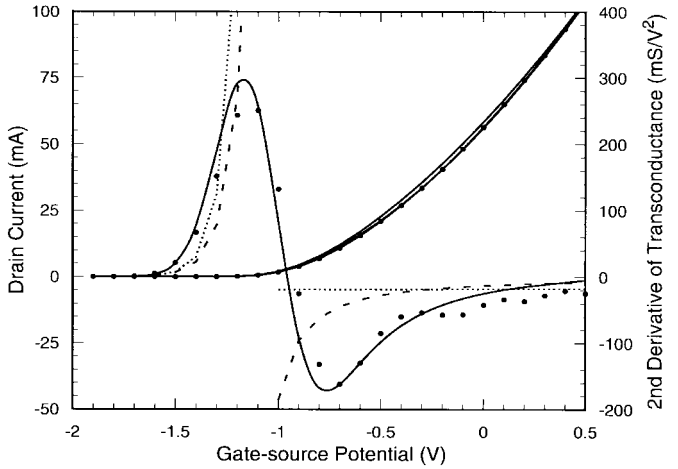

Fig. 4. Saturated drain current and its third derivative described by three different models: Statz *et al.* [2] (· · · · · ·) and McCamant *et al.* [3] (- - -) with exponential subthreshold regions, and the new model (——). Measured data at $v_{\rm DS} = 2$ V (•) is also shown.

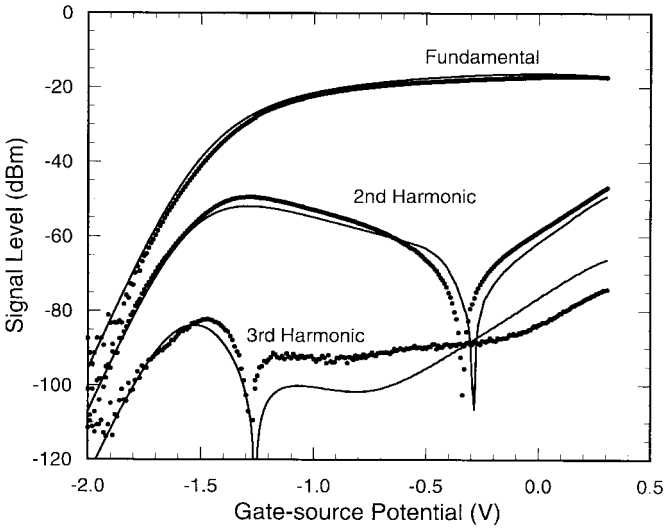

Fig. 5. Measured (•) and simulated (——) fundamental and second and third harmonic output products from a 1-μm MESFET operating in common-source configuration with 50-Ω source and load impedances. Results are for -24 dBm input tones at 40 and 60 MHz and a 2-V drain bias.

harmonic distortion of a typical MESFET. The simulated results predict the general structure of the distortion variation with bias.

D. Drain Conductance

In the controlled-current mode, the drain current rises with increasing drain potential. In short-channel FET's, this effect is an apparent modulation of the pinchoff potential. In this model, the effective gate–source potential relative to the channel pinchoff potential includes modulation by the bias gate–drain potential

$$v_{\rm GST} = v_{\rm GS} - V_{TO} - \gamma_{\rm lf}\overline{v_{\rm GD}}. \tag{9}$$

The dc description is similar to other models that modulate the pinchoff potential with the drain–source potential. Gate–drain modulation was chosen for this model for consistency with the description of frequency dispersion.

The pinchoff potential V_{TO} and model parameters β and P are best determined from measurements in the controlled-resistance region, near zero drain–source potential. A successful procedure is to extract the pinchoff potential using the Fukui method [21], then fit β and P to (6).

Substituting $V_{\rm sat}$ for $v_{\rm DT}$ in (2) and then $v_{\rm GST}$ given by (9) for $v_{\rm GT}$ approximates the drain current description in the controlled-current mode. The term $\gamma_{\rm lf}$ in (9), noting that $v_{\rm GD} = v_{\rm GS} - v_{\rm DS}$, is then seen to be the ratio of drain conductance $G_d = di_D/dv_{\rm DS}$ to transconductance $g_{mi} = di_D/dv_{\rm GS}$:

$$\gamma_{\rm lf} = \frac{G_d}{G_d + g_{mi}} \approx \frac{G_d}{g_{mi}}. \tag{10}$$

There are three model parameters, $LF_{\rm GAM}$, $LF_{\rm G1}$, and $LF_{\rm G2}$ that set this ratio as a function of gate–source and gate–drain bias potentials as follows:

$$\gamma_{\rm lf} = LF_{\rm GAM} - LF_{\rm G1}\overline{v_{\rm GS}} + LF_{\rm G2}\overline{v_{\rm GD}}. \tag{11}$$

IV. Frequency Dispersion

Rate-dependent anomalies in short-channel MESFET's are well known [22] and produce differences between drain conductance at dc and at high frequencies. The model describes this effect by responding to high-frequency deviations from an established operating point.

A. Drain Conductance and Transconductance

The effective gate–source potential is redefined in terms of the following instantaneous and bias potentials:

$$v_{\rm GST} = v_{\rm GS} - V_{TO} - \gamma_{\rm lf}\overline{v_{\rm GD}} - \gamma_{\rm hf}(v_{\rm GD} - \overline{v_{\rm GD}}) - \eta_{\rm hf}(v_{\rm GS} - \overline{v_{\rm GS}}). \tag{12}$$

The model determines the bias condition by a continuous calculation of the average value of the terminal potentials as follows:

$$\overline{v_{\rm GS}} = v_{\rm GS} - \tau_G \frac{d}{dt}\overline{v_{\rm GS}}$$
$$\overline{v_{\rm GD}} = v_{\rm GD} - \tau_G \frac{d}{dt}\overline{v_{\rm GD}}. \tag{13}$$

This allows the model to respond to variations in bias during a time-domain simulation. The average is accumulated over a user-defined time constant, τ_G, which is normally between 0.1–1 ms.

The SPICE implementation of (13) uses state variables in a finite-difference calculation of the averages [11]. The average potential at time t is calculated by a weighted sum of the instantaneous potential at time t and the previously calculated average at time $t - \Delta t$ as follows:

$$\overline{v(t)} = v(t) + (\overline{v(t - \Delta t)} - v(t))e^{-\Delta t/\tau}. \tag{14}$$

The term v here is either $v_{\rm GS}$ or $v_{\rm GD}$ as required, and the present time t and time step Δt are provided by the simulator when it calls the model code.

At very low frequencies, the instantaneous and average potentials are identical, so (12) reduces to (9).

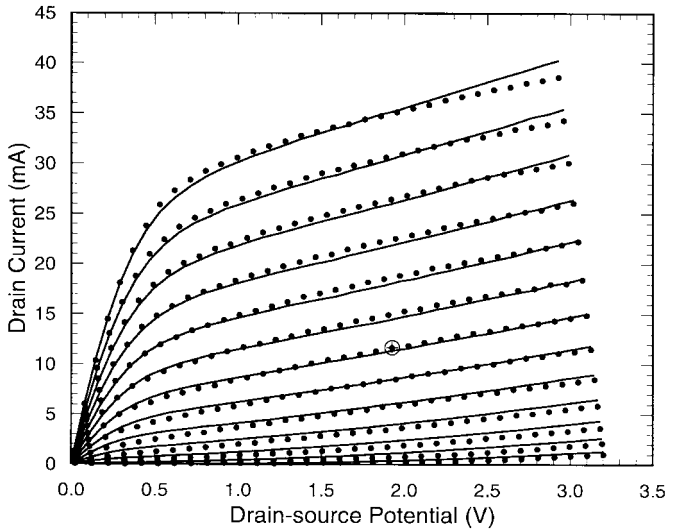

Fig. 6. Pulsed-bias measured (•) and simulated (—) *I–V* characteristics of a MESFET. The operating point (2 V, 12 mA) is shown by ⊕. Gate–source potential, from −1.2 to 0 V in 0.1-V steps, is a parameter.

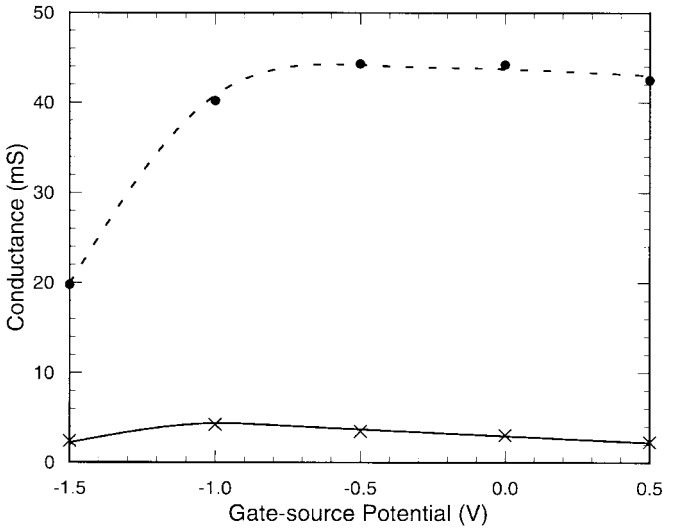

Fig. 7. Transconductance (- - -) and drain–conductance (——) derived from S-parameter measurements of a typical MESFET at $v_{\rm DS} = 4$ V. Measurements are also shown (•, ×).

At high frequency, the average potentials remain constant, so the terms $\gamma_{\rm lf}$ and $\eta_{\rm hf}$ have an effect. The drain conductance is increased by a factor $\gamma_{\rm hf}/\gamma_{\rm lf}$ and the transconductance is reduced by a factor $(1-\gamma_{\rm hf}-\eta_{\rm hf})/(1-\gamma_{\rm lf})$. The model adjusts this high-frequency dispersion with bias using six model parameters ($HF_{\rm GAM}$ to $HF_{\rm E2}$) as follows:

$$\gamma_{\rm hf} = HF_{\rm GAM} - HF_{\rm G1}\overline{v_{\rm GS}} + HF_{\rm G2}\overline{v_{\rm GD}}$$
$$\eta_{\rm hf} = HF_{\rm ETA} - HF_{\rm E1}\overline{v_{\rm GD}} + HF_{\rm E2}\overline{v_{\rm GS}}. \qquad (15)$$

The terms $\gamma_{\rm hf}$ and $\eta_{\rm hf}$ can be determined from the ratio of measured high-frequency conductances to those predicted by the low-frequency model. High-frequency drain conductance and transconductance can be extracted from S-parameter data [23], or from measurements at tens of megahertz, or from pulsed *I–V* data. Fig. 6 shows a typical simulation of pulse-derived characteristics that exhibit increased drain conductance. Fig. 7 shows extracted and simulated conductances obtained from S-parameter data.

Separation of drain conductance and transconductance dispersion provides much better simulation of small-signal behavior. Two feedback potentials provide a significant improvement over models that use the average drain–source potential [13]–[15]. The new model can simulate the characteristic complexity observed in a curve-tracer measurement [22]. An example of this is shown in Fig. 8.

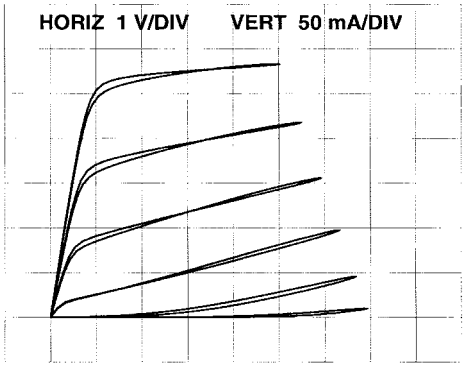

Fig. 8. Simulated curve-tracer display for a typical MESFET. The shape requires both source–gate feedback and drain–gate feedback.

B. Power Dissipation

Power dissipated in the FET channel will inevitably give a temperature increase with a corresponding reduction in channel conductivity. The model describes this by scaling drain current with a function of average power dissipation. A useful correction for junction heating is based on [3] as follows:

$$i_{\rm DS} = \frac{i_D}{1+\delta P}. \qquad (16)$$

The term δ is a model parameter related to the product of the temperature coefficient of current reduction and the channel thermal resistance. The model calculates average dissipated power rather than using instantaneous power. The calculation is over a time constant τ_D using the algorithm of (14):

$$P = i_D v_{\rm DS} - \tau_D \frac{d}{dt} P. \qquad (17)$$

The thermal time constant is a realistic feature omitted from many models. This omission in these models tends to balance their lack of transconductance dispersion. The two feedback potentials in the new model allow it to separate the dispersion and heating effects correctly. This provides a much better simulation of small-signal operation.

The ratio of dc drain conductance $G_{\rm ds} = di_{\rm DS}/dv_{\rm DS}$ to dc transconductance $g_m = di_{\rm DS}/dv_{\rm GS}$ is a relatively simple function in controlled-current mode, where subthreshold conduction can be ignored:

$$\frac{G_{\rm ds}}{g_m} = \gamma_{\rm lf} - \delta\frac{i_{\rm DS}^2}{g_m}. \qquad (18)$$

Measurements of this ratio at low frequency can be used to extract δ.

V. Charge Storage Model

Describing capacitance in a circuit simulator, such as SPICE, is complicated because the charges on the source and drain are not state variables of FET operation. Despite this, the simulator must maintain total charge conservation in order to avoid convergence problems [24]. In this model, gate charge is defined by terminal potentials and is balanced by source and drain charges. The model is an enhanced description based on [2], implemented to conserve charge following [24]. This provides a suitable description even though the partition of charge between source and drain is not explicitly defined.

A. Gate–Source Capacitance

Total gate charge $Q_{\rm gg}$ is controlled by model parameters $C_{\rm GS}$ and $C_{\rm GD}$ respectively, which are the gate–source capacitance at zero gate–source potential and the gate–drain capacitance

$$Q_{\rm gg} = 2C_{\rm GS}\phi_b\left(1-\sqrt{1-V_{\rm new}/\phi_b}\right)+C_{\rm GD}V_{\rm eff2}. \quad (19)$$

This function uses two effective potentials, $V_{\rm new}$ and $V_{\rm eff2}$, which in controlled-current mode, are the gate–source and gate–drain potentials, respectively. In this mode the gate–drain capacitance, found by differentiation with respect to gate–drain potential, is $C_{\rm GD}$.

The effective gate–source potential calculation of [2] is used with a new parameter to add gate–source fringing capacitance

$$V_{\rm new} = V_{\rm eff1}X_C + \tfrac{1}{2}(1-X_C)(V_{\rm eff1}+V_{TO} + \sqrt{(V_{\rm eff1}-V_{TO})^2+(0.2/(1-X_C))^2}). \quad (20)$$

In controlled-current mode, $V_{\rm eff1}$ is the gate–source potential. When this potential is large, $V_{\rm new}$ becomes $v_{\rm GS}$ and the gate–source capacitance follows a standard depletion capacitance description

$$C_{\rm gs} = \frac{C_{\rm GS}}{\sqrt{1-v_{\rm GS}/\phi_b}}. \quad (21)$$

In cutoff mode, $V_{\rm new}$ becomes $X_C(v_{\rm GS}-V_{TO})+V_{TO}$ and the capacitance is reduced by factor X_C, rather than to zero:

$$C_{\rm gs} = \frac{X_C C_{\rm GS}}{\sqrt{1-V_{\rm new}/\phi_b}}. \quad (22)$$

B. Forward Gate Bias

Control over forward-bias junction capacitance is provided with parameter F_C. When $V_{\rm new} > F_C\phi_b$, the gate–source capacitance is made a linear function of gate–source potential. In this condition, the model switches to an alternative description of gate charge as follows:

$$Q_{\rm gg} = C_{\rm GS}\phi_b\left\{2(1-\sqrt{1-F_C})+\frac{(V_{\rm new}/\phi_b-F_C)^2}{4(1-F_C)^{3/2}} + \frac{V_{\rm new}/\phi_b-F_C}{(1-F_C)^{1/2}}\right\}+C_{\rm GD}V_{\rm eff2}. \quad (23)$$

Fig. 9 shows the improved prediction of gate–source capacitance obtained with these enhancements.

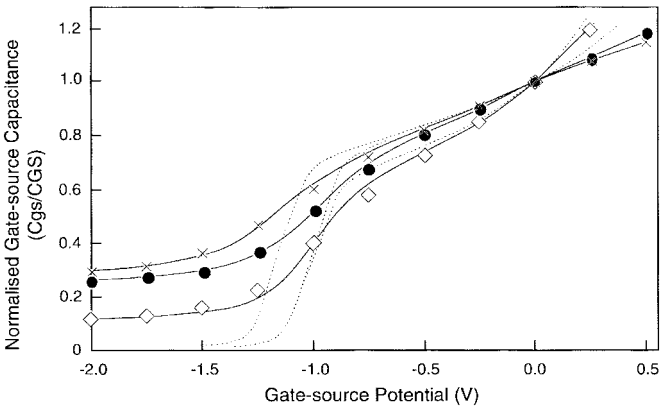

Fig. 9. Experimental intrinsic gate–source capacitance data from various MESFET's at $v_{\rm DS} = 1.5$ V. The corresponding modified capacitance model is shown by solid lines. The original model is shown by dashed lines.

C. Gate–Drain Capacitance

Bias dependence is also added to the capacitance model. The effective potentials of [2] are modulated with the new parameter $\gamma_{\rm AC}$ as follows:

$$V_{\rm eff1} = \tfrac{1}{2}(v_{\rm GS}+v_{\rm GD}+\sqrt{v_{\rm DS}^2+\alpha^2})+\gamma_{\rm AC}v_{\rm DS}$$
$$V_{\rm eff2} = \tfrac{1}{2}(v_{\rm GS}+v_{\rm GD}-\sqrt{v_{\rm DS}^2+\alpha^2})+\gamma_{\rm AC}v_{\rm DS}. \quad (24)$$

These functions facilitate a reversal of charge when the source and drain potentials swap. This occurs over a region defined by α, which is related in this model to the drain potential at the knee between controlled-resistance and controlled-current modes

$$\alpha = \frac{\xi}{\xi+1}\,\frac{\phi_b-V_{TO}}{2}. \quad (25)$$

The effect of $\gamma_{\rm AC}$ in the controlled-current mode is to give the gate–drain capacitance some dependence on $v_{\rm GS}$ as follows:

$$C_{gd} = C_{\rm GD}(1-\gamma_{\rm AC})-\gamma_{\rm AC}\frac{C_{\rm GS}}{\sqrt{1-v_{\rm GS}/\phi_b}}. \quad (26)$$

This capacitance model is adequate for predicting S-parameters. Fig. 10 shows a typical set of S-parameter curves over various bias conditions. Fig. 11 shows simulated and measured S_{21} from a similar device. Overall, small-signal performance of the model is illustrated in Fig. 12. This shows the accuracy of predicted S-parameters over a wide range of bias conditions. Note that the simulation is accurate at $v_{\rm DS} = 0$ and in the subthreshold region. The error near the saturation knee of the device is a consequence of sensitivity to the rapid changes in S_{22}, rather than any increased error in the model.

VI. Implementation

The model presented here is an extended JFET description that incorporates velocity saturation in a general power law. The model is a general device description valid for long- and short-channel noninsulated-gate FET's. It includes second-order effects that are important in short-channel GaAs MESFET's. Dispersion of transconductance, drain conductance, and heating due to power dissipation are modeled.

TABLE I
SPICE MODEL PARAMETERS FOR THE NEW MESFET MODEL

Name	Description	Default	Units	Example	Area	Symbol
ACGAM	Capacitance modulation	0	-	0.11		γ_{AC}
BETA	Linear-region transconductance scale	10^{-4}	$A \cdot V^{-Q}$	0.30	×	β
CGD	Zero-bias gate-source capacitance	0	F	200fF	×	C_{GD}
CGS	Zero-bias gate-drain capacitance	0	F	820fF	×	C_{GS}
DELTA	Thermal reduction coefficient	0	W^{-1}	0.1	÷	δ
FC	Forward bias capacitance parameter	0.5	-	0.3		F_C
HFETA	High-frequency v_{GS} feedback parameter	0	-	0.10		HF_{ETA}
HFE1	HFGAM modulation by V_{GD}	0	V^{-1}	0.05		HF_{E1}
HFE2	HFGAM modulation by V_{GS}	0	V^{-1}	0.17		HF_{E2}
HFGAM	High-frequency VGD feedback parameter	0	-	0.09		HF_{GAM}
HFG1	HFGAM modulation by V_{SG}	0	V^{-1}	0.06		HF_{G1}
HFG2	HFGAM modulation by V_{DG}	0	V^{-1}	0.01		HF_{G2}
IBD	Gate-junction breakdown current	0	A	800p	×	I_{BD}
IS	Gate-junction saturation current	10^{-14}	A	1.1p	×	I_S
LFGAM	Low-frequency feedback parameter	0	-	0.03		LF_{GAM}
LFG1	LFGAM modulation by V_{SG}	0	V^{-1}	0.008		LF_{G1}
LFG2	LFGAM modulation by V_{DG}	0	V^{-1}	0.0		LF_{G2}
MVST	Subthreshold modulation	0	V^{-1}	0.04		M_{VST}
N	Gate-junction ideality factor	1	-	1.15		N
P	Linear-region power-law exponent	2	-	2.4		P
Q	Saturated-region power-law exponent	2	-	2.0		Q
RS	Source ohmic resistance	0	Ω	0.7	÷	R_S
RD	Drain ohmic resistance	0	Ω	1	÷	R_D
TAUD	Relaxation time for thermal reduction	0	s	10u		τ_D
TAUG	Relaxation time for gamma feedback	0	s	1m		τ_G
VBD	Gate-junction breakdown potential	1	V	1.2		V_{BD}
VBI	Gate-junction potential	1	V	0.8		ϕ_b
VST	Subthreshold potential	0	V	0.07		V_{ST}
VTO	Threshold voltage	–2.0	V	–1.5		V_{TO}
XC	Capacitance pinch-off reduction factor	0	-	0.2		X_C
XI	Saturation-knee potential factor	1000	-	0.18		ξ
Z	Knee transition parameter	0.5	-	0.34		Z

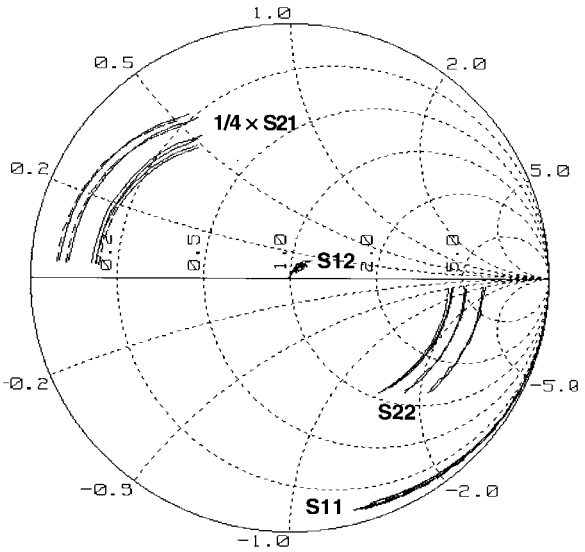

Fig. 10. Measured (——) and simulated (- - -) S-parameters from 0.5 to 6 GHz of a typical MESFET at four bias points in the controlled-current operating mode ($v_{\rm DS} = 1$ and 2 V and $v_{\rm GS} = -1$ and 0 V).

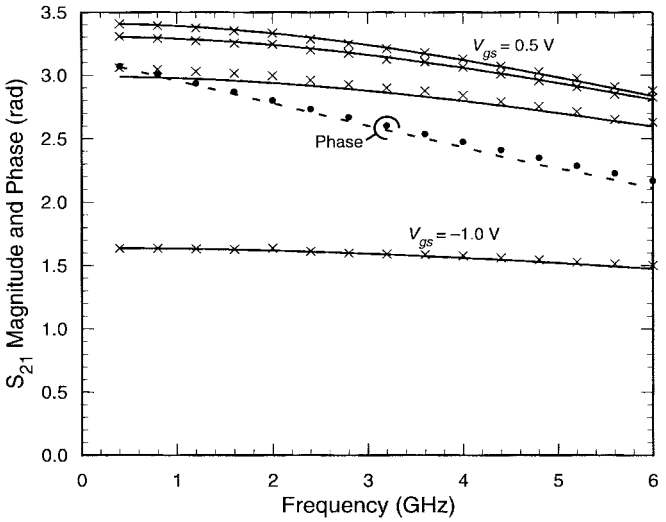

Fig. 11. Measured and simulated S_{21} for a typical MESFET biased at $v_{\rm DS} = 4$ V. Each line is for $v_{\rm GS} = -1.0, -0.5, 0.0$, and 0.5 volts. Both magnitude (×) and phase (•) are shown.

The implementation in SPICE3f4 sets default model parameter values that preserve the original SPICE JFET model. The JFET temperature-dependence model, which affects the built-in and pinchoff potentials, is retained. The additional short-channel effects of the model are activated simply by using the appropriate model parameters. Gate ohmic resistance can be added, but it should be noted that a single area factor is not adequate for multifingered devices. Table I lists the parameters used in the SPICE implementation.

In summary, the SPICE model implements the circuit of Fig. 1. The intrinsic drain–source current element is given

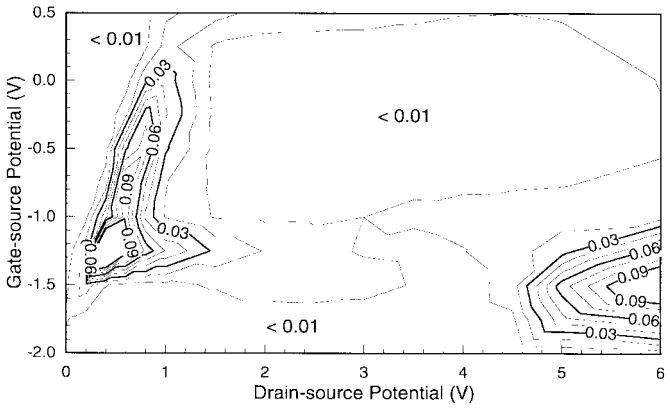

Fig. 12. Absolute-square error in simulated S-parameters of a MESFET referenced to measurements at 2 GHz. Pinchoff is at -1.5 V. The error function is the sum of squares of differences between simulation and measurement, $\Sigma|S_{ij}^m - S_{ij}^s|^2$.

TABLE II
SUMMARY OF THE INTRINSIC DRAIN–CURRENT MODEL

The terms i_{DS}, v_{GS}, v_{GD}, and v_{DS} are as in Fig. 1. Other variables are model parameters listed in table I.

$$i_{DS} = \frac{i_D}{1+\delta P}$$

where

$$P = i_D v_{DS} - \tau_D \, dP/dt$$

and

$$i_D = \beta v_{GT}^Q \left[1 - (1 - v_{DT}/v_{GT})^Q\right]$$

with

$$\begin{aligned}
v_{GT} &= V_{ST}(1 + M_{VST} v_{DS}) \\
&\quad \cdot \ln\left(1 + \exp\left(\frac{v_{GST}}{V_{ST}(1 + M_{VST} v_{DS})}\right)\right) \\
v_{GST} &= v_{GS} - V_{TO} - \gamma_{lf}\,\overline{v_{GD}} \\
&\quad -\gamma_{hf}\,(v_{GD} - \overline{v_{GD}}) - \eta_{hf}\,(v_{GS} - \overline{v_{GS}}) \\
\gamma_{lf} &= LF_{GAM} - LF_{G1}\,\overline{v_{GS}} + LF_{G2}\,\overline{v_{GD}} \\
\gamma_{hf} &= HF_{GAM} - HF_{G2}\,\overline{v_{GS}} + HF_{G2}\,\overline{v_{GD}} \\
\eta_{hf} &= HF_{ETA} - HF_{E1}\,\overline{v_{GD}} + HF_{E2}\,\overline{v_{GS}} \\
\overline{v_{GS}} &= v_{GS} - \tau_G\, d\overline{v_{GS}}/dt \\
\overline{v_{GD}} &= v_{GD} - \tau_G\, d\overline{v_{GD}}/dt \\
v_{DT} &= \frac{1}{2}\sqrt{\left(v_{DP}\sqrt{1+Z} + V_{sat}\right)^2 + Z V_{sat}^2} \\
&\quad -\frac{1}{2}\sqrt{\left(v_{DP}\sqrt{1+Z} - V_{sat}\right)^2 + Z V_{sat}^2} \\
v_{DP} &= v_{DS}\frac{P}{Q}\left(\frac{v_{GT}}{\phi_b - V_{TO}}\right)^{P-Q} \\
V_{sat} &= \xi(\phi_b - V_{TO})\, v_{GT}/(\xi(\phi_b - V_{TO}) + v_{GT})
\end{aligned}$$

TABLE III
SUMMARY OF THE GATE-CHARGE MODEL

The terms v_{GS}, v_{GD}, and v_{DS} are as in Fig. 1. Other variables are model parameters listed in table I.

If $V_{new} \le F_C \phi_b$

$$Q_{gg} = 2C_{GS}\phi_b\left(1 - \sqrt{1 - V_{new}/\phi_b}\right) + C_{GD}V_{eff2}$$

If $F_C\phi_b < V_{new}$

$$\begin{aligned}
Q_{gg} &= C_{GS}\phi_b\left\{2\left(1 - \sqrt{1-F_C}\right) + \frac{(V_{new}/\phi_b - F_C)^2}{4(1-F_C)^{3/2}}\right. \\
&\quad \left. + \frac{V_{new}/\phi_b - F_C}{(1-F_C)^{1/2}}\right\} + C_{GD}V_{eff2}
\end{aligned}$$

where

$$\begin{aligned}
V_{new} &= V_{eff1}X_C + \frac{1}{2}(1 - X_C)\left(V_{eff1} + V_{TO}\right. \\
&\quad \left. + \sqrt{\left(V_{eff1} - V_{TO}\right)^2 + (0.2/(1-X_C))^2}\right)
\end{aligned}$$

$$\begin{aligned}
V_{eff1} &= \frac{1}{2}\left(v_{GS} + v_{GD} + \sqrt{v_{DS}^2 + \alpha^2}\right) + \gamma_{AC}v_{DS} \\
V_{eff2} &= \frac{1}{2}\left(v_{GS} + v_{GD} - \sqrt{v_{DS}^2 + \alpha^2}\right) + \gamma_{AC}v_{DS}
\end{aligned}$$

$$\alpha = \frac{\xi}{\xi+1}\,\frac{\phi_b - V_{TO}}{2}$$

in Table II, which summarizes equations (5), (7), (11)–(13), (15)–(17). The gate–drain and gate–source diodes are described by (1). The gate–drain and gate–source capacitances are the differential of (19) and (23), which use (20), (24), and (25), and are summarized in Table III.

The model has been implemented with strict consistency between the basic SPICE analysis types. The small-signal ac model is a correct representation of the large-signal transient analysis model at any dc bias. The rate dependency of the large-signal model is implemented as frequency dependence in the ac model. This provides very good agreement with RF measurement. In addition, the model is symmetrical with respect to drain–source potential. The transition during drain–source potential reversal is smooth and continuous.

Despite the model's sophistication, it runs up to five times faster than simpler descriptions that do not use the nested transformation scheme. The improvement is due to the overall continuity of the model, which permits rapid convergence. Also, average potentials are accumulated in state variables rather than at extra nodes in the simulator [11].

VII. CONCLUSION

The comprehensive MESFET model presented in this paper is accurate over an extended range of operating conditions. It features high-order continuity for realistic prediction of intermodulation and improved convergence speed. The model has sufficient detail to predict high-frequency S-parameters over all bias points. The model has been implemented in various industry-standard simulators including those by University of California at Berkeley (SPICE 3f4), EEsof, MicroSim, Anacad, and Intusoft. Source code for SPICE3F4 implementation is available via the Internet [25].

The new model is a valuable tool for the design of modern communications circuits. A single characterization is valid for various operating modes encountered in microwave cir-

cuits. Descriptions of the controlled-resistance and controlled-current regions use independent power laws. Its rate dependency adapts the model to any bias condition. Transconductance and drain-conductance dispersion occur during high-frequency excursions around the bias point. This gives correct small-signal S-parameters in any bias region, including the controlled-resistance region. A thermal time constant controls response to power dissipation. There is no requirement for a suite of model parameters.

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REFERENCES

[1] W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 448–456, May 1980.
[2] H. Statz, P. Newman, I. W. Smith, R. A. Pucel, and H. A. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 160–169, Feb. 1987.
[3] A. J. McCamant, G. D. McCormack, and D. H. Smith, "An improved GaAs MESFET model for SPICE," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 822–824, June 1990.
[4] A. Materka and T. Kacprzak, "Computer calculation of large-signal GaAs FET amplifier characteristics," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 129–135, Feb. 1985.
[5] W. R. Curtice and M. Ettenberg, "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 1383–1394, Dec. 1985.
[6] J. Conger, M. S. Shur, and A. Peczalski, "Power law GaAs MESFET model," *IEEE Trans. Electron Devices*, vol. 39, pp. 2415–2417, Oct. 1992.
[7] J. M. Golio, J. R. Hauser, and P. A. Blakey, "A large-signal GaAs MESFET model implemented on SPICE," *IEEE Circuits Devices Mag.*, vol. 1, pp. 21–30, Sept. 1985.
[8] V. K. De and J. D. Meindl, "Three-region analytical models for MESFET's in low-voltage digital circuits," *IEEE J. Solid-State Circuits*, vol. 26, pp. 850–858, June 1991.
[9] C. C. Enz, "The EKV model: A MOST model dedicated to low-current and low-voltage analogue circuit design and simulation," in *Low-Power HF Microelectronics: A Unified Approach*, G. A. S. Machado, Ed. London, U.K.: IEE, 1996, ch. 6, pp. 247–300.
[10] I. Angelov, H. Zirath, and N. Rorsman, "A new empirical nonlinear model for HEMT and MESFET devices," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2258–2266, Dec. 1992.
[11] A. E. Parker, "Implementing high-order continuity and rate dependence in SPICE models," *Proc. Inst. Elect. Eng. Circuits, Devices, and Syst.*, vol. 141, pp. 251–257, Aug. 1994.
[12] A. E. Parker and D. J. Skellern, "Improved MESFET characterization for analog circuit design and analysis," in *IEEE GaAs IC Symp. Tech. Digest*, Miami Beach, FL, Oct. 4–7 1992, pp. 225–228.
[13] C. Camacho-Peñalosa and C. S. Aitchison, "Modeling frequency dependence of output impedance of a microwave MESFET at low frequencies," *Electron. Lett.*, vol. 21, no. 12, pp. 528–529, June 1985.
[14] N. Scheinberg, R. J. Bayruns, and R. Goyal, "A low-frequency GaAs MESFET circuit model," *IEEE J. Solid-State Circuits*, vol. 23, pp. 605–608, Apr. 1988.
[15] J. M. Golio, M. G. Miller, G. N. Maracas, and D. A. Johnson, "Frequency-dependent electrical characteristics of GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. 37, pp. 1217–1227, May 1990.
[16] R. A. Pucel, H. A. Haus, and H. Statz, "Signal and noise properties of gallium arsenide microwave field-effect transistors," in *Advances in Electronics and Electron Physics*, L. Marton, Ed. New York: Academic, 1975, vol. 38, pp. 195–265.
[17] W. Shockley, "A unipolar 'field-effect' transistor," *Proc. IRE*, vol. 40, pp. 1365–1376, 1952.
[18] C. T. M. Chang, T. Vrotsos, M. T. Frizzel, and R. Carroll, "A subthreshold current model for GaAs MESFET's," *IEEE Electron Device Lett.*, vol. EDL-8, pp. 69–72, Feb. 1987.
[19] J. Conger, A. Peczalski, and M. Shur, "Subthreshold current in GaAs MESFET's," *IEEE Electron Device Lett.*, vol. 9, pp. 128–129, Mar. 1988.
[20] S. A. Maas and D. Neilson, "Modeling GaAs MESFET's for intermodulation analysis," *Microwave J.*, vol. 34, no. 5, pp. 295–300, May 1991.
[21] H. Fukui, "Determination of the basic device parameters of a GaAs MESFET," *Bell System Tech. J.*, vol. 58, no. 3, pp. 771–797, Mar. 1979.
[22] P. H. Ladbrooke and S. R. Blight, "Low-field low-frequency dispersion of transconductance in GaAs MESFET's with implications for other rate-dependent anomalies," *IEEE Trans. Electron Devices*, vol. 35, pp. 257–267, Mar. 1988.
[23] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151–1159, July 1988.
[24] I. W. Smith, H. Statz, H. A. Haus, and R. A. Pucel, "On charge nonconservation in FET's," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 2565–2568, Dec. 1987.
[25] (1996). *SPICE Circuit Simulator*. [Online]. Available: URL: http://www.mpce.mq.edu.au/elec/cnerf/spice/ and also available FTP: mpce.mq.edu.au/pub/elec/spice/.

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